Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) Method of operating a driving circuit for a display system, wherein the sequence of writing and/or reading video data into and/or from a memory is controlled by means of an address sequencer, each of the memory addresses for said video data generated in the address sequencer being composed of a picture line address part or line pointer and an address part for a pixel on said picture line, the method comprising:

operating the driving circuit alternately in a first mode wherein the address sequencer generates addresses for the video data in the memory by combining line pointers that are read out by a line counter from a block of line pointers in address table register means with the output of a pixel counter using an adder~~counting means~~, and in a second mode wherein a block of line pointers from a full table of line pointers in said memory is downloaded into said address table register means.

2. (currently amended) Driving circuit for a display system comprising:

a memory for video data to be displayed and coupled thereto an address sequencer for controlling the sequence of writing and/or reading the video data in said memory, characterized in that the memory contains a full table of line pointers, each line pointer being part of a memory address for video data, and in that the address sequencer is provided with address table register means for a block of line pointers from said table of line pointers;

means for successively updating the address table register means with subsequent blocks of line pointers;

a pixel counter~~counting means~~, the output of which in combination with the consecutive line pointers that are read out by a line counter from the address table register means using an adder determines the addresses for said video data; and

switching means, by which alternately memory addresses for video data are generated in a first mode in the address sequencer, and in a second mode the address table register is updated with a next block of line pointers.

3. (canceled)

4. (previously presented) Driving circuit as claimed in claim 2, characterized in that the memory comprises a full table of line pointers for different sequences of video data to be displayed.

5. (previously presented) Apparatus for displaying images comprising a display system and a driving circuit according to claim 2.

6. (canceled)

7. (previously presented) A computer readable medium that stores a computer program capable of running on signal processing means in a driving circuit for a display system according to claim 2.

8. (canceled)

9. (currently amended) Driving circuit for a display system comprising:

a memory for video data to be displayed and coupled thereto an address sequencer for controlling the sequence of writing and/or reading the video data in said memory, characterized in that the memory contains a full table of line pointers for different sequences of video data to be displayed, each line pointer being part of a memory address for video data, and in that the address sequencer is provided with address table register means for a block of line pointers from said table of line pointers;

means for successively updating the address table register means with subsequent blocks of line pointers; and

a pixel counter~~counting means~~, the output of which in combination with the consecutive line pointers that are read out by a line counter from the address table register means using an adder determines the addresses for said video data.

10. (previously presented) A computer readable medium that stores a computer program capable of running on signal processing means in an apparatus for displaying images according to claim 5.

11. (new) The method of claim 1, wherein each block of line pointers is limited to thirty two line pointers.

12. (new) Driving circuit as claimed in claim 2, wherein the number of line pointers in the address table register means is limited to thirty two.

13. (new) Driving circuit as claimed in claim 9, wherein the number of line pointers in the address table register means is limited to thirty two.